JCG60R180S

Product Preview

600V 180mΩ Superjunction MOSFET

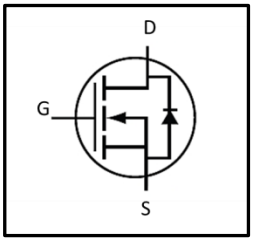
Features

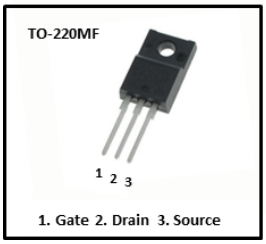
- Advanced superjunction technology
- Ultra-low on-resistance and gate-charge
- RoHS compliant
- 100% avalanche tested

Product Summary	
V_{DS}	600 V
$R_{DS(ON)}$	150 mΩ (Typ.)
	180 mΩ (Max.)
I_D	19 A

Applications

- Server/PC
- Telecom
- LED Applications





Ordering Information

Part Number	Marking	Package	Packaging
JCG60R180S	CG60R180S	TO-220MF	Tube

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Drain-to-Source Voltage	V_{DSS}	600	V
Gate-to-Source Voltage	V_{GSS}	±30	V
Continuous Drain Current, Silicon Limited (T_C = 25°C) (1),(2)	I_D	19	A
Continuous Drain Current, Silicon Limited (T_C = 100°C) (1),(2)	I_D	12	A
Pulsed Drain Current (3)	I_{DM}	57	A
Avalanche Energy, Single Pulse (4)	E_{AS}	76	mJ
Power Dissipation (T_C = 25°C)	P_D	36	W
Avalanche Current (4)	I_{AS}	4	A
Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	

Thermal Characteristics

Parameter	Symbol	Max	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	62.5	°C/W
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	3	

Static Electrical Characteristics (5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA	600	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS} , I_D = 1.7 mA	2.5	-	4.5	
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V	-	-	±100	nA
Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 8.5 A	-	150	180	mΩ
Gate Resistance	R_G	f = 1 MHz, open drain	-	1.3	-	Ω

Dynamic Electrical Characteristics (5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total Gate Charge	Q_g	V_{GS} = 10 V,	-	31	-	nC
Gate-to-Source Charge	Q_{gs}	V_{DS} = 400 V,	-	6	-	
Gate-to-Drain Charge	Q_{gd}	I_D = 8.5 A	-	16	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V,	-	12	-	ns
Rise Time	t_r	V_{DS} = 400 V,	-	8	-	
Turn-Off Delay Time	$t_{d(off)}$	I_D = 8.5 A,	-	53	-	
Fall Time	t_f	R_G = 10 Ω	-	10	-	
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 250 kHz,	-	1240	-	pF
Output Capacitance	C_{oss}	V_{DS} = 400 V	-	34	-	
Reverse Transfer Capacitance	C_{rss}			3		
Effective Output Capacitance, Energy Related (6)	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 400 V		54		pF
Effective Output Capacitance, Time Related (7)	$C_{o(tr)}$	V_{GS} = 0 V, V_{DS} = 0 V to 400 V		381		pF

Source Drain Characteristics (5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_F = 8.5 A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	V_R = 400 V,	-	274	-	ns
Reverse Recovery Charge	Q_{rr}	I_F = 8.5 A,	-	4	-	μC
Peak Reverse Recovery Current	I_{rrm}	di_F/dt = 100 A/us	-	-	-	A

(1) Limited by maximum $T_{J\,max}$. Maximum duty cycle D=0.75.

(2) Rated according to $R_{\theta JA}$.

(3) Repetitive rating: pulse-width limited by maximum junction temperature.

(4) T_A = 25°C, R_G = 25Ω, I_{AS} = 4 A.

(5) T_J = 25°C unless otherwise specified.

(6) $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is changing from 0 to 400 V.

(7) $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is changing from 0 to 400 V.

Electrical Characteristics Diagrams

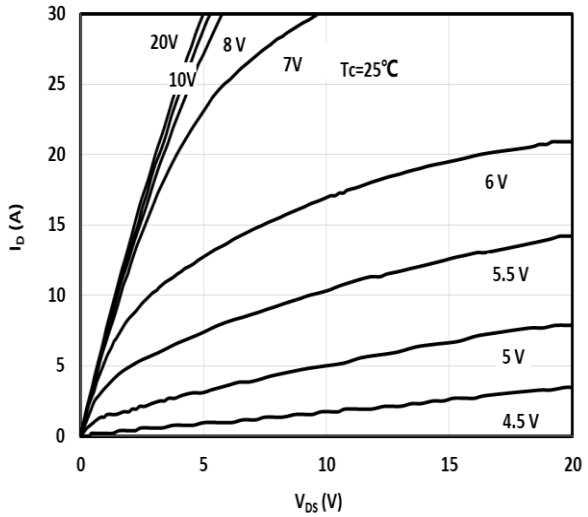


Fig. 1 Typical output characteristics

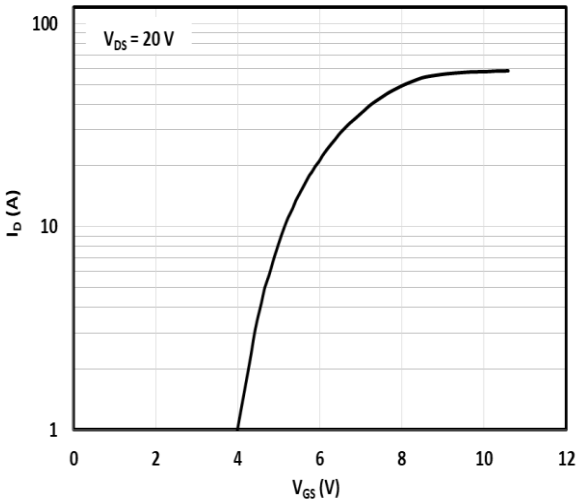


Fig. 2 Typical transfer characteristics

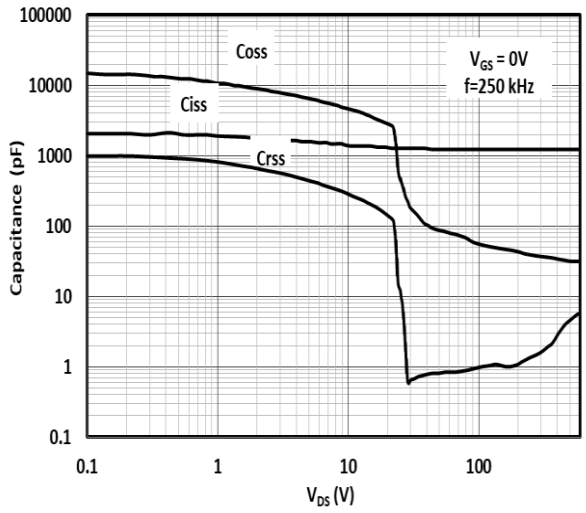


Fig. 3 Typical capacitance characteristics

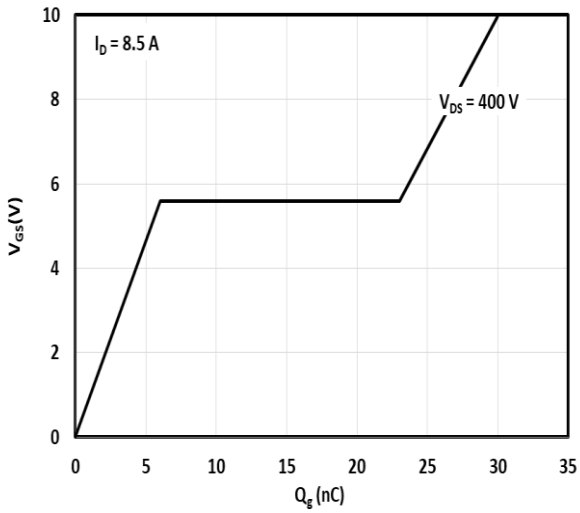


Fig. 4 Typical gate charge characteristics

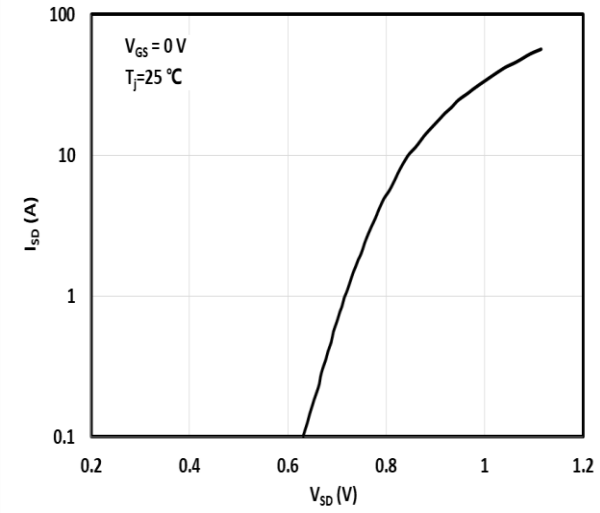


Fig. 5 Typical forward characteristics of body diode

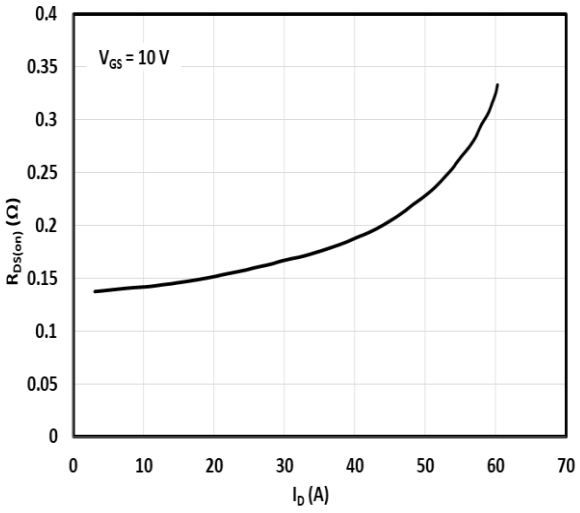


Fig. 6 Typical drain-source on-state resistance

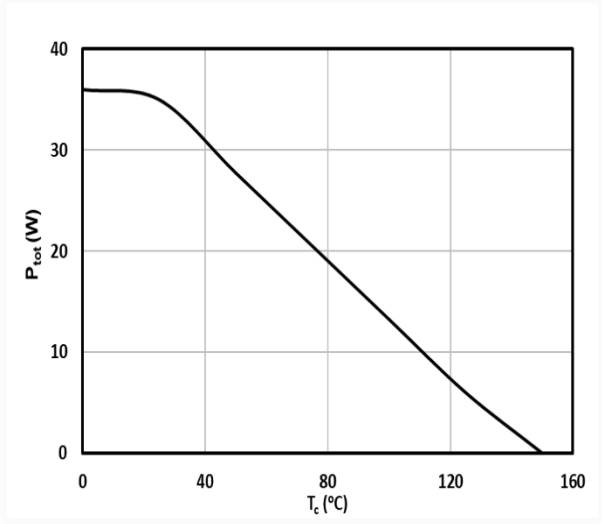


Fig. 7 Typical power dissipation

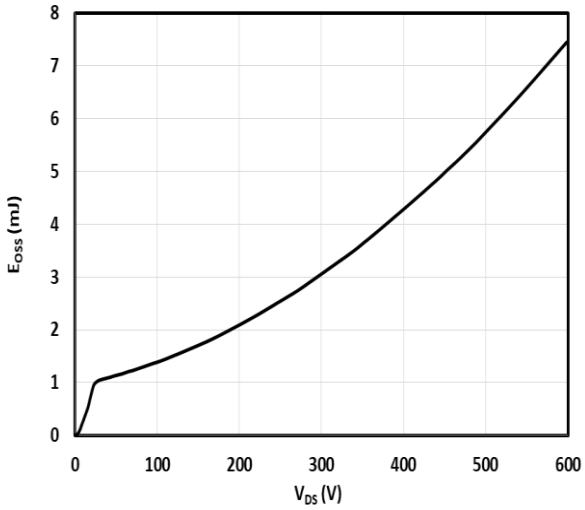


Fig. 8 Typical C_{oss} stored energy

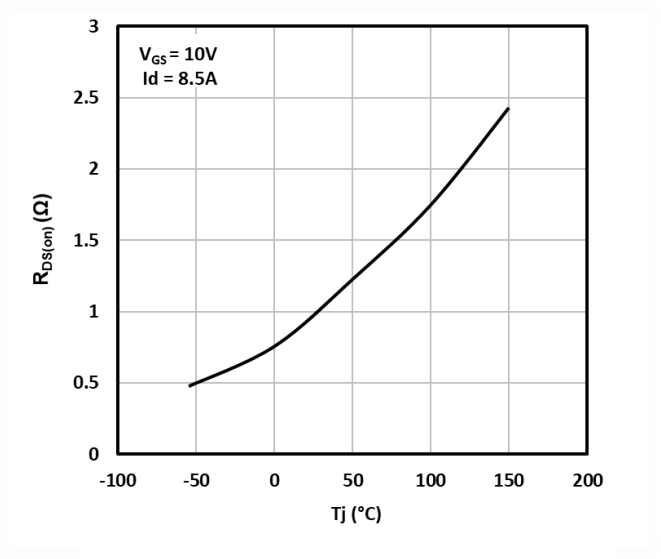


Fig. 9 On-resistance Characteristics vs. Temperature

Test Circuits and Waveforms

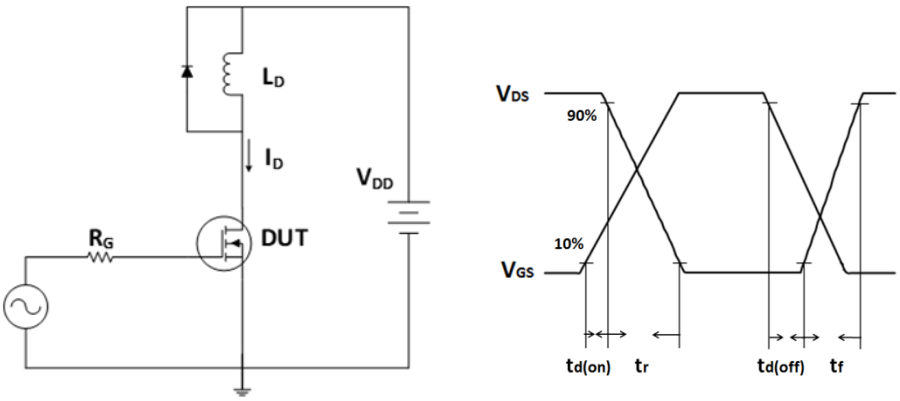


Fig. 1 Inductive switching time test circuit & waveforms

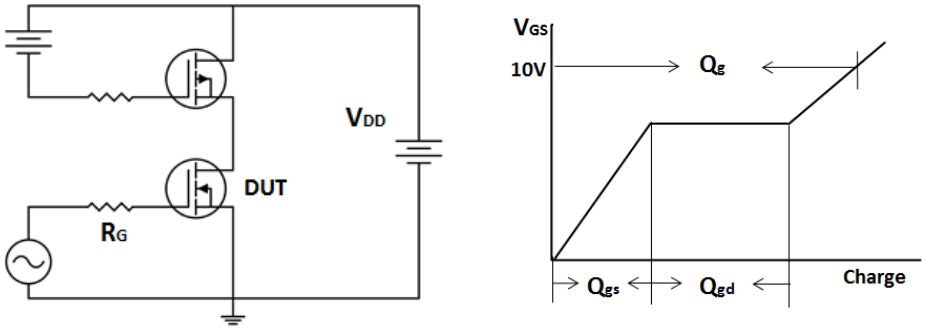


Fig. 2 Gate charge test circuit & waveform

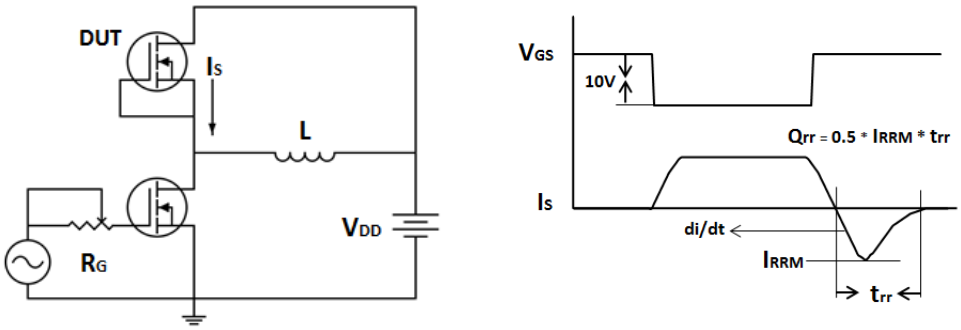


Fig. 3 Peak diode recovery dv/dt test circuit & waveforms

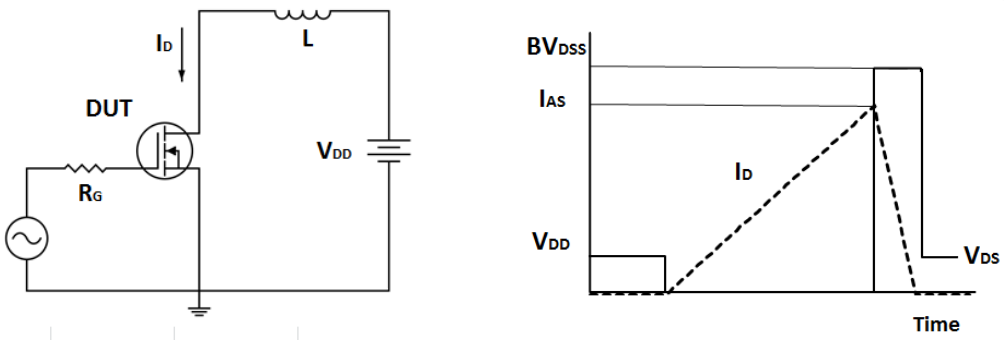
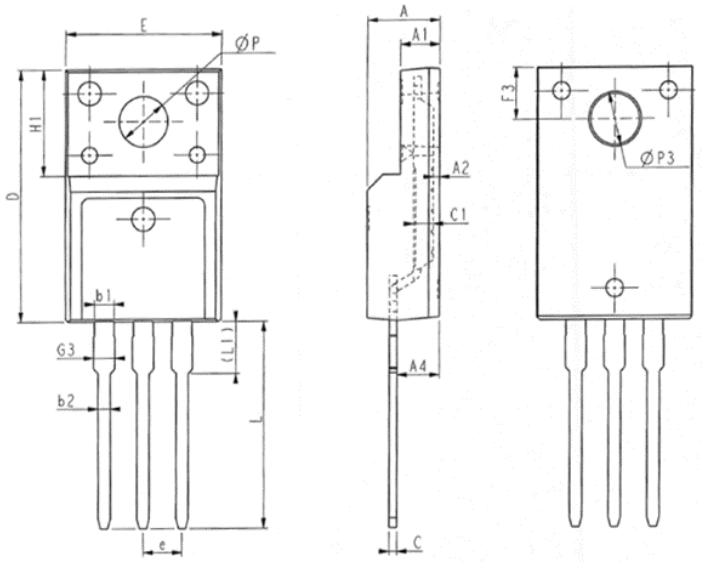


Fig. 4 Unclamped inductive switching test circuit & waveforms

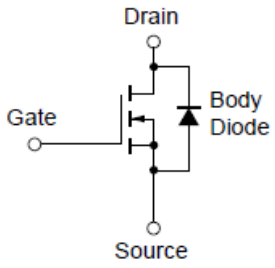
Package Drawing



SYMBOL	MM		
	MIN	NOM	MAX
E	9.96	10.16	10.36
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	0.30	0.45	0.60
A4	2.56	2.76	2.96
c	0.40	0.50	0.65
c1	1.20	1.30	1.35
D	15.57	15.87	16.17
H1	6.70REF		
e	2.54BSC		
L	12.68	12.98	13.28
L1	3.03	3.23	3.43
ΦP	3.03	3.18	3.38
ΦP3	3.15	3.45	3.65
F3	3.15	3.30	3.45
G3	1.25	1.35	1.55
b1	1.18	1.28	1.43
b2	0.70	0.80	0.95

TO-220MF

Equivalent Circuit



Revision history of JCG60R180S specification

Version	Change Items	Effective Date
1.00	Initial release.	12-Jan-22

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